

FIG. 2

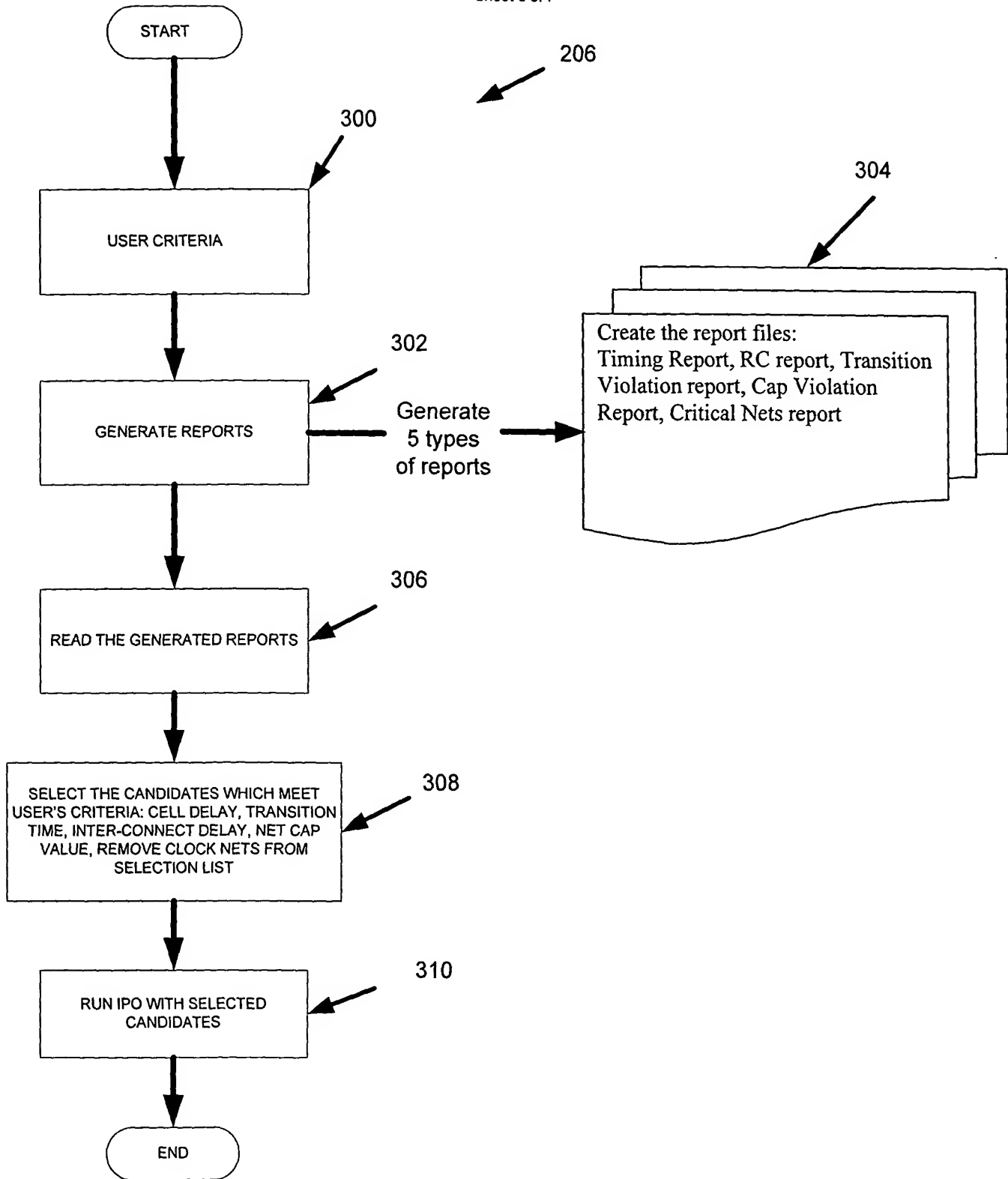
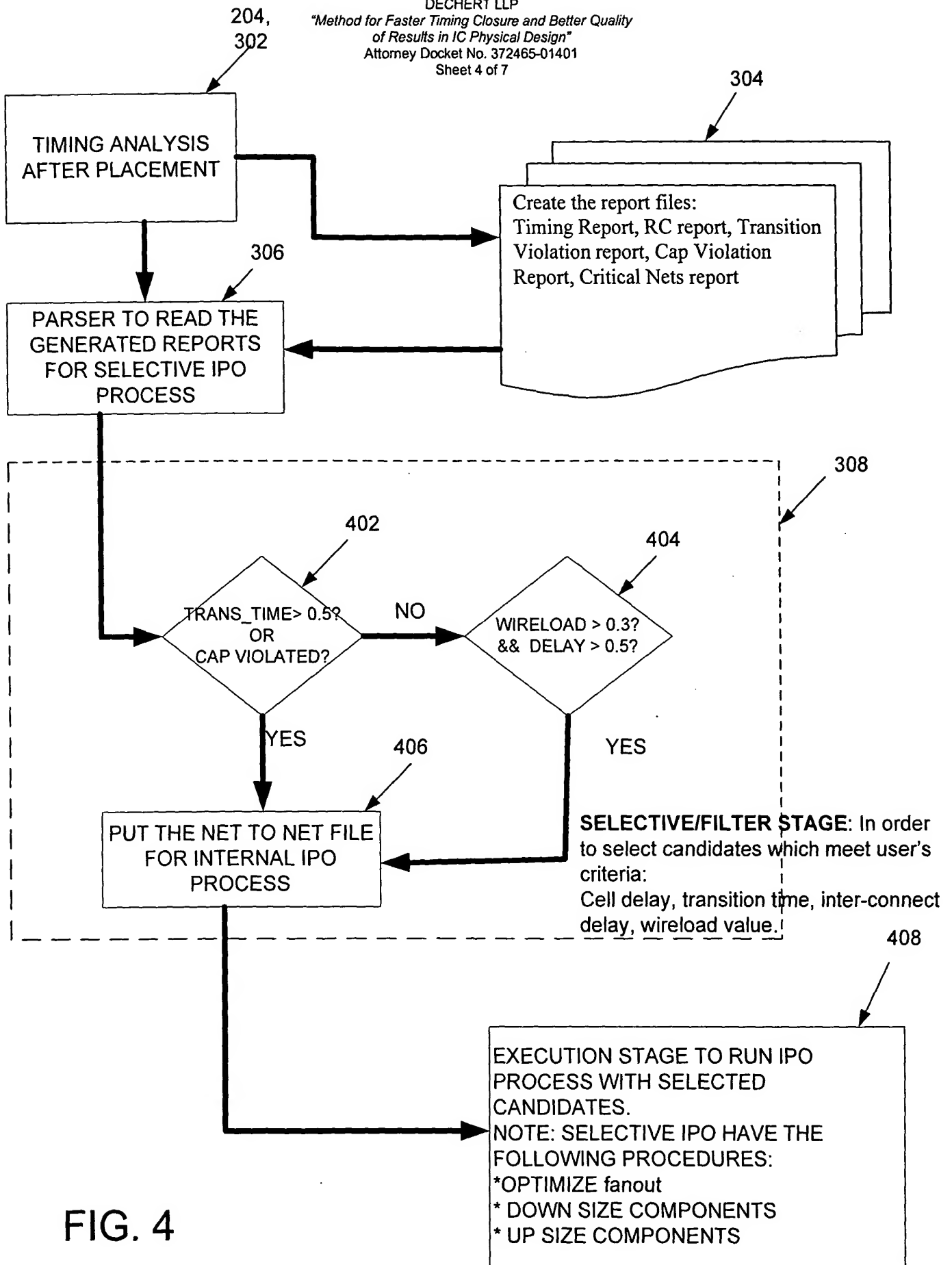


FIG.3



## Capacitance Violation File

# InstPin #	MaxCap	Cap	CapSlack	CellPort
i_meu/ibiu_i_inst/U1217/Y	0.171	0.898	-0.727	BUFX2TH/Y
i_meu/miu_i_inst/U6094/Y	1.024	1.743	-0.719	BUFX12TH/Y
i_meu/U1/Y	0.085	0.796	-0.711	INVX1TH/Y
i_meu/biu_i_inst/U1215/Y	0.341	1.042	-0.701	BUFX4TH/Y
i_meu/biu_i_inst/U1230/Y	0.171	0.870	-0.699	BUFX2TH/Y
i_meu/biu_i_inst/U1207/Y	0.341	1.039	-0.698	BUFX4TH/Y

FIG. 5A

## Transition timing report

# InstPin	MaxTranTime	TranTime	TranSlack	CellPort
i_bci/u_bcif/U416/A	1.500	11.272r/6.066f	-9.772r/-4.566f	NAND2X1TH/A
i_meu/U1/Y	1.500	11.272r/6.066f	-9.772r/-4.566f	INVX1TH/Y
i_bci/u_parsch/U1046/A0	1.500	11.272r/6.066f	-9.772r/-4.566f	AO22X1TH/A0
i_reg_cntrl/U29/Y	1.500	11.003r/4.024f	-9.503r/-2.524f	NOR2BX1TH/Y
i_reg_cntrl/TIME/D1	1.500	11.003r/4.024f	-9.503r/-2.524f	SMDFFHQX1TH/D1
i_reg_cntrl/FSM/U12/Y	1.500	10.955r/4.010f	-9.455r/-2.510f	NOR2X1TH/Y
i_bci/mio_read/U351/Y	1.500	10.628r/2.944f	-9.128r/-1.444f	NOR4X1TH/Y

FIG. 5B

## Critical Net report

i\_vs/i\_alu/i\_source\_sel/SPCDPN13319\_n2584  
 i\_vs/i\_alu/i\_source\_sel/SPCDPN13318\_n2647  
 i\_vs/i\_alu/i\_source\_sel/SPCDPN13317\_n2549  
 i\_vs/i\_alu/i\_source\_sel/SPCDPN13316\_n2547  
 i\_vs/i\_alu/i\_vector\_even/i\_muladd\_vec/SPCDPN13310\_n38174  
 i\_thiu/TIS\_FFCTL/SPCDPN13292\_n455  
 i\_vs/i\_alu/i\_source\_sel/SPCDPN13268\_n4692  
 i\_thiu/PROC\_2D/U\_th\_2d\_img\_seq/SPCDPN13263\_n5244

FIG. 5C

## Timing Analysis report file

### Object name

Delta r/f (ns)	Sum r/f (ns)	Slew (ns)	Load (pf)	Cell Location (um)
INST1 CK->Q (SDFFRHQX8TH)				
0.320f/0.346r	0.320f/0.346r	0.120f/0.120r	0.110	(1291.22, 1380.06)
INST2 A->Y (BUFX20TH)				
0.208f/0.235r	0.529f/0.582r	0.190f/0.210r	0.426	(1293.52, 1376.37)
INST3 B->Y (NAND2X4TH)				
0.099r/0.089f	0.632r/0.675f	0.230f/0.313r	0.005	(1259.94, 1372.68)

FIG. 5D

### Selective IPO Netfile

i\_vs/i\_alu/i\_source\_sel/n4132  
i\_vs/i\_alu/i\_source\_sel/n4063  
i\_vs/i\_alu/i1\_seta/SPCDPN4239\_x0\_odd\_18\_  
i\_vs/i\_alu/i\_source\_sel/n4092  
i\_vs/i\_alu/i0\_float\_fix/n53  
i\_vs/i\_alu/n1447  
i\_vs/i\_alu/n1448

FIG. 5E

## IPO command file

```
genIPONets $CellDelay $OutputTransition $NetCap
setIPOMode -mediumEffort -noFixDrc -addPortAsNeeded -noPreserveRoute \
-targetSlack 0 -maxDensity 0.90 -selHInst {} -exchInst {}
optFanout -selNetFile .netFile
trialRoute
extractRC
updateTimingGraph

genIPONets $CellDelay $OutputTransition $NetCap
setAnalysisMode -setup -async -noSkew -autoDetectClockTree
updateTimingGraph

setIPOMode -mediumEffort -noFixDrc -addPortAsNeeded -noPreserveRoute \
-targetSlack 0 -maxDensity 0.90 -selHInst {} -exchInst {}
initECO
updateTimingGraph

isTimingMet -fast -targetSlack 0.0
setIPOMode -preserveRoute
downsize -selNetFile .netFile
resize -selNetFile .netFile
setIPOMode -noPreserveRoute
extractRC
updateTimingGraph

isTimingMet -fast -targetSlack 0.0
optFanout -selNetFile .netFile
trialRoute
extractRC
updateTimingGraph

isTimingMet -fast -targetSlack 0.0
upsized -selNetFile .netFile
trialRoute
extractRC
updateTimingGraph

cleanupECO
savedesign $my_design.enc
```

FIG. 6